## REMARKS

Claims 1-26, and 41-43 are now pending. Claims 27-40 are cancelled in response to a Restriction Requirement issued by the USPTO on June 7, 2005. Claims 1-3, 5-9, 11-13, 15-16, 18-20, and 24-25 are amended. Claims 41-43 are added. No new matter is added as a result of the above amendments. Reconsideration of presently pending claims 1-26 is respectfully requested in light of the above amendments and the following remarks.

### Objection to Specification

The Examiner objects to the specification because of the informalities on page 1 of the specification. By this Response, amendments have been made to the specification to delete a reference to related patent application, docket no. 2002-1068, which is now abandoned.

### Rejections Under 35 U.S.C. §112, Second Paragraph, Claims 1-12, and 18-26

Claims 1-12 and 18-26 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner alleges that the phrases in claims 1-12 and 18-26 are vague, indefinite, and awkwardly worded. By this Response, amendments have been made to claims 1-3, 5-9, 11-12, 18-20, and 24-25 to remove the limitation "or" and to positively recite each claim limitation. Accordingly, Applicants respectfully request the withdrawal of the rejections to claims 1-12 and 18-26 under 35 U.S.C. §112, second paragraph.

### Allowable Subject Matter, Claims 4, 6-10, 12, 16, 17-23, and 25

Applicants thank Examiner Wilson for the indication of allowable subject matter in claims 4, 6-10, 12, 16, 17-23, and 25. However, for the reasons set forth hereafter, Applicants respectfully submit that all of the claims are directed to allowable subject matter and that the application is in condition for allowance.

**Rejections Under 35 U.S.C. §102(b), Claims 1-3, 5, 11, 13-15. 24 and 26**

Claims 1-3, 5, 11, 13-15, 24 and 26 are rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Toprac (US Patent No. 6,884,147 hereinafter referred to as "Toprac").

Amended independent claim 1 now recites:

> 1. An advanced process control (APC) method for a target layer polish process in a polish tool that minimizes within wafer and wafer to wafer sheet resistance (Rs) variations in a plurality of wafers having a metal layer formed on a barrier layer within an opening in a dielectric layer, said metal layer has a thickness, width, and cross-sectional area, comprising:
>
> providing a plurality of wafers each having a metal layer that has been formed on a barrier layer within an opening in a dielectric layer by a sequence of processing steps;
>
> determining a relationship between the cross-sectional area of said metal layer and Rs;
>
> determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process;
>
> determining a target layer polish thickness target for said metal layer on each of said plurality of wafers; and
>
> calculating a target layer polish time for each of said plurality of wafers in the target layer polish process. (Emphasis added).

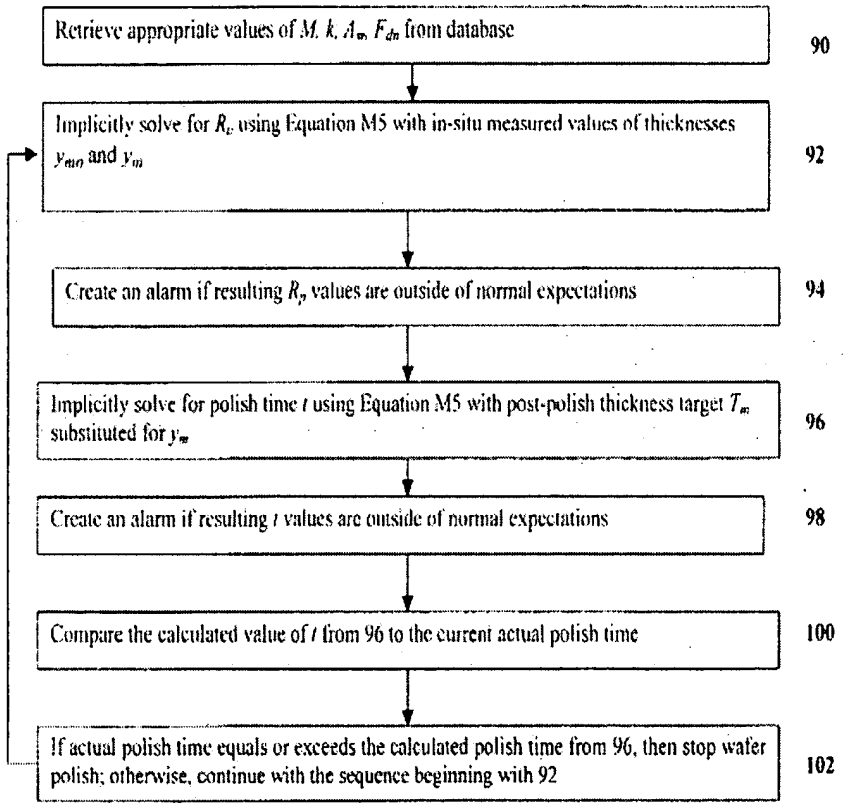
The PTO provides in MPEP § 2131 that

> *"[t]o anticipate a claim, the reference must teach every element of the claim...."*

Therefore, with respect to claims 1 and 13, to sustain this rejection the Toprac patent must contain all of the above claimed elements of the claim. However, contrary to the Examiner's position that all elements are disclosed in the Toprac reference, the latter reference does not disclose determining a relationship between the cross-sectional area of said metal layer and Rs, or determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process.

The Examiner alleges that Toprac discloses the same process which may not have the same equation but shows the same final results. The equational process is being read as a way of producing the process without all of the hard equations. Applicants respectfully disagree.

Toprac fails to disclose the same process as alleged by the Examiner. Fig. 5 of the Toprac is shown below:




As shown in Fig. 5 and at column 12, line 40 to column 13, line 50, Toprac discloses a real-time CMP control method for production wafer polish. The method first retrieves M, constant k, wafer area $A_w$, and $F_{dn}$, the downforce value set in the polish recipe, from a database. A wafer polish rate $R_p$ is solved using a equation as determined wit in-situ measured thickness used for $y_{m0}$ and $y_m$. If $R_p$ is outside of normal expectations, an alarm is created. Next, a polish time t is determined with the post polish thickness target $T_m$ substituted for $y_m$ and an alarm is created if the resulting t values are outside of the normal expectations. The value of t is

compared to the current actual polish time. If the actual polish time equals or exceeds the calculated polish time, wafer polish stops. Otherwise, the process continues.

However, nowhere in the reference does Toprac mention anything about Rs, which is within wafer and wafer to wafer sheet resistance, let alone determining a relationship between the cross-sectional area of said metal layer and Rs. Toprac is only interested in determining a wafer polish rate $R_p$ and determining whether the polish rate is within normal expectations. Toprac is not interested in Rs. In addition, since Toprac is not interested in Rs, Toprac does not and would not disclose determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process. Therefore, Toprac fails to disclose the feature of claims 1 and 13 of the present disclosure.

Therefore, the rejection is not supported by the Toprac reference and should be withdrawn.

Claims 1-3, 5, 11, 13-15, 24 and 26 are rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Williams (US Patent No. 6,594,542 hereinafter referred to as "Williams").

Similar to Toprac, Williams also does not disclose determining a relationship between the cross-sectional area of said metal layer and Rs, or determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process, as recited in claim 1. At column 4, lines 48-61, Williams discloses "a method for controlling thickness removal of a substrate during polishing of a series of n substrates...to include: measuring a thickness of a first substrate prior to polishing, polishing the first substrate for a predetermined time; measuring the thickness of the first substrate after polishing; determining an actual thickness removal rate, based on the measurement before, the measurement after, and the predetermined time; and applying a linear estimation factor, based on the actual thickness removal rate, to form an adjusted polishing time for a subsequent substrate to be polished, to adjust for degradation and inconsistency of a polishing surface that occurs during the polishing of multiple substrates."

Williams also fails to mention anything about within wafer and wafer to wafer sheet resistance (Rs). Williams is only interested in determining an actual thickness removal rate and

adjusts the polishing time based on the rate. Therefore, Williams does not and would not disclose Rs, let alone determining a relationship between the cross-sectional area of said metal layer and Rs, or determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process. Therefore, Williams also fails to disclose the features of claims 1 and 13 of the present disclosure.

Therefore, the rejection is not supported by the Williams reference and should be withdrawn.

Claims 1-3, 5, 11, 13-15, 24 and 26 are rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Meikle, et al. (US Patent No. 5,655,951 hereinafter referred to as "Meikle").

As discussed in the Abstract, Meikle discloses "a method for selectively reconditioning a polishing pad used in the chemical-mechanical planarization of semiconductor wafers. A desired polishing rate is selected based upon a set of operating parameters. A desired change in the thickness of the pad material is estimated for reconditioning the pad to achieve a desired polishing rate. The estimate of the desired change in the pad thickness is based upon the desired polishing rate and predetermined correlation between wafer polishing rates and changes in the pad thickness per conditioning cycle. A layer of material having a thickness substantially equal to the desired change in thickness is then removed from the planarizing surface to create a new planarizing surface."

Thus, similar to Toprac and Williams, Meikle is only concerned with a desired polishing rate rather than a within wafer and wafer to wafer sheet resistance, Rs. In addition, nowhere in the reference does Meikle mention anything about Rs, let alone determining a relationship between the cross-sectional area of said metal layer and Rs, or determining a total Rs ($Rs_{TOTAL}$) for the metal layer on each of said plurality of wafers before said target layer polish process. Therefore, Meikle also fails to disclose the features of claims 1 and 13 of the present disclosure.

Therefore, the rejection is not supported by the Meikle reference and should be withdrawn.

**Conclusion**

It is clear from all of the foregoing that independent claims 1 and 13 are in condition for allowance. Dependent claims 2-12, 14-26, and 41-43 from and further limit independent claims 1 and 13 and therefore are allowable as well.

An early formal notice of allowance of claims 1-26 and 41-43 is requested.

Respectfully submitted,

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